UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,646	01/05/2005	Laurent Clavelier	034299-616	5193

7590 09/07/2006

Thelen Reid & Priest
P O Box 640640
San Jose, CA 95164-0640

EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/520,646	CLAVELIER ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 11-16 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Sopori (5,897,331).

2. Regarding claim 1, Sopori discloses an electronic device (Figure 3, reference 4) comprising an active part (Figure 3, reference 9), a first thin layer which is made of a semiconductor material and in which this active part is formed (Figure 3, reference 1), and a substrate made of an electrically conductive material (Figure 3, reference 3), this device being characterized in that it also comprises a carrier recombination zone which is located between the substrate and the first thin layer and which also ensures a resistive electric contact between this substrate and this first thin layer (Figure 3, reference 2).

3. Regarding claim 2, Sopori discloses wherein the carrier recombination zone is a second thin layer which is made of an electrically conductive material and which ensures electrically conductive bonding between the substrate and the first thin layer (Figure 3, reference 2).

4. Regarding claim 3, Sopori discloses wherein the two sides of the first thin layer are treated to form active zones of the device (column 9, lines 40-60; *electromagnetic radiation*).

5. Regarding claim 4, Sopori discloses wherein the material in which the carrier recombination zone is made is a metal (Figure 3, reference 2).

6. Regarding claim 5, Sopori discloses wherein the material in which the carrier recombination zone is made is a semiconductor/metal alloy (column 8, lines 66-67 thru column 9, lines 1-5).

7. Regarding claim 6, Sopori discloses wherein the alloy in which the carrier recombination zone is made is chosen so that it is stable with respect to the materials in which the substrate and the first thin layer are respectively made (column 8, lines 66-67 thru column 9, lines 1-31).

8. Regarding claim 7, Sopori discloses wherein the material in which the substrate is made is a highly doped semiconductor, in particular highly doped silicon (column 3, lines 38-61; column 9, lines 5-11).

9. Regarding claim 8, Sopori discloses wherein the material in which the carrier recombination zone is made is a metal and this metal is chosen so that, when fabricating the resistive electric contact, it forms a stable alloy with the highly doped semiconductor in which the substrate is made and with the semiconductor material in which the first thin layer is made (column 8, lines 66-67 thru column 9, lines 1-31).

10. Regarding claim 11, Sopori discloses a process for fabricating an electronic device, this process being characterized in that it comprises the following steps: part of the device is formed in a standard semiconductor substrate, on the front side of this standard

semiconductor substrate, a treatment support is fixed to the front side of the substrate, the standard semiconductor substrate is thinned via its rear side, so as to transform said substrate into a thin layer, another part of the device is formed in the standard semiconductor substrate so transformed, on the rear side of this standard semiconductor substrate, on the rear side of this standard semiconductor substrate and/or on a side of an electrically conductive substrate, a thin layer is deposited formed of a metal or of a metal/semiconductor alloy, via the thin layer formed of the metal or metal/semiconductor alloy, electrically conductive bonding is carried out between the electrically conductive substrate and the thin layer into which the standard semiconductor substrate was transformed, and the treatment support is removed (column 8, lines 66-67 thru column 9, lines 1-31).

11. Regarding claim 12, Sopori discloses a process for fabricating an electronic device, this process being characterized in that it comprises the following steps: part of the device is formed in a standard semiconductor substrate, on the rear side of this standard semiconductor substrate, on the rear side of this standard semiconductor substrate and/or on a side of an electrically conductive substrate, a thin layer is deposited formed of a metal or a metal/semiconductor alloy, electrically conductive bonding is carried out between the electrically conductive substrate and the standard semiconductor substrate, via the thin layer, the standard semiconductor substrate is thinned via its front side so as to transform said substrate into a thin layer, and another part of the device is formed in the standard semiconductor substrate so transformed, on the front side of this standard semiconductor substrate (column 8, lines 66-67 thru column 9, lines 1-31).

12. Regarding claim 13, Sopori discloses wherein electric contacts of the device are also formed on the thin layer in which the standard semiconductor substrate was transformed, and on the electrically conductive substrate (column 8, lines 66-67 thru column 9, lines 1-9).

13. Regarding claim 14, Sopori discloses wherein the electrically conductive substrate is made of a material chosen from among highly doped semiconductors in particular highly doped silicon, and conductors in particular metals (column 3, lines 51-54; column 8, lines 66-67 thru column 9, lines 1-9).

14. Regarding claim 15, Sopori discloses wherein the electrically conductive substrate is made of a material chosen from among highly doped semiconductors, in particular highly doped silicon, the metal or the metal/semiconductor alloy being chosen so that, after annealing subsequent to electrically conductive bonding, it forms a stable alloy with the material in which the electrically conductive substrate is made and with the material in which the standard semiconductor substrate is made (column 8, lines 66-67 thru column 9, lines 1-31).

15. Regarding claim 16, Sopori discloses wherein the electrically conductive bonding step is preceded by a preparative step to prepare at least one of the two sides to be assembled by electrically conductive bonding, so as to promote this bonding (column 3, lines 28-61).

16. Regarding claim 18, Sopori discloses wherein electric contacts of the device are also formed on the thin layer in which the standard semiconductor substrate was transformed, and on the electrically conductive substrate (column 8, lines 66-67 thru column 9, lines 1-9).

17. Regarding claim 19, Sopori discloses wherein the electrically conductive substrate is made of a material chosen from among highly doped semiconductors in particular highly

doped silicon, and conductors in particular metals (column 3, lines 51-54; column 8, lines 66-67 thru column 9, lines 1-9).

18. Regarding claim 20, Sopori discloses wherein the electrically conductive substrate is made of a material chosen from among highly doped semiconductors, in particular highly doped silicon, the metal or the metal/semiconductor alloy being chosen so that, after annealing subsequent to electrically conductive bonding, it forms a stable alloy with the material in which the electrically conductive substrate is made and with the material in which the standard semiconductor substrate is made (column 8, lines 66-67 thru column 9, lines 1-31).

19. Regarding claim 21, Sopori discloses wherein the electrically conductive bonding step is preceded by a preparative step to prepare at least one of the two sides to be assembled by electrically conductive bonding, so as to promote this bonding (column 3, lines 28-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sopori (5,897,331) in view of Ishikawa et al (US 2005/0095842 A1).

20. Sopori discloses all above claimed subject matter except the substrate is made of metal (claims 9 and 10) and the recombination zone is made in the metal in which the substrate is made and is formed by part of this substrate (claim 10)

Ishikawa et al discloses the substrate is made of metal (pg.5, paragraph 0064) and the recombination zone is made in the metal in which the substrate is made and is formed by part of this substrate (Figure 1A).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Sopori with the teachings of Ishikawa et al for the purpose of forming a reliable multi-layer wiring structure.

Claims 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sopori (5,897,331) in view of Bhat et al (US 2003/0205712).

21. Sopori et al discloses all above claimed subject matter except electrically conductive bonding is chosen from among bonding by soldering, bonding by thermal compression and bonding by molecular adhesion (claims 17 and 22).

Bhat et al discloses electrically conductive bonding is chosen from among bonding by soldering, bonding by thermal compression and bonding by molecular adhesion (pg.1, paragraph 0003).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Sopori with the teachings of Bhat et al for the purpose of forming an electrical connection between the layers by using solder bumps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Monica D. Harrison
AU 2813

mdh
September 1, 2006

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800